WHAT IS CLAIMED IS:

1. A method for generating a test vector for functional verification of circuits comprising:

providing a representation of a circuit, the representation comprising a control logic component and a datapath logic component;

reading one or more vector generation targets;

performing word-level ATPG justification on the control logic component to obtain a control logic solution;

extracting one or more arithmetic functions for the datapath logic component based on the control logic solution; and

solving the one or more arithmetic functions using a modular constraint solver, the modular constraint solver being based on a modular number system.

2. The method of Claim 1, wherein the word-level ATPG justification comprises performing word-level implication on circuit components related to the one or more targets.

3. The method of Claim 1, wherein solving the one or more arithmetic functions comprises:

determining possible solutions for the one or more nonlinear equations; and

solving the one or more linear equations using one possible solution for the one or more nonlinear equations as boundary conditions.

4. The method of Claim 1 further comprising:

dependent on the outcome of solving the one or more arithmetic functions, backtracking to perform word-level ATPG justification on the control logic component to obtain a second control logic solution;

extracting one or more arithmetic functions for the datapath logic component based on the second control logic solution; and

solving the one or more arithmetic functions using the modular constraint solver.

5. The method of Claim 1, wherein the vector generation target comprises a signal value.

6. The method of Claim 1, wherein the vector generation target comprises a relation among a set of signals.

7. The method of Claim 1, wherein the vector generation target comprises a sequence of relations among a set of signals.

8. A method for performing word-level ATPG justification on a target circuit, the target circuit comprising one or more control signals, the method comprising:

identifying an internal control signal of the target circuit;

making a decision on the identified internal control signal;

performing word-level implication on circuit components related to the target circuit;

determining if a conflict arises from the word-level implication; and

determining if the one or more control signals are justified.

9. The method of Claim 8 further comprising:

in response to determining that a conflict arose, backtracking to the previous decision on the identified internal control signal; and

undoing the word-level implication associated with the previous decision.

10. The method of Claim 8 further comprising:

in response to determining that the one or more control signals are not justified, identifying a second internal control signal of the target circuit;

making a decision on the identified second internal control signal;

performing word-level implication on circuit components related to the target circuit;

determining if a conflict arises from the word-level implication; and

determining if the one or more control signals are justified.

11. A method for performing word-level ATPG on a target circuit, the target circuit comprising one or more control signals and one or more data signals, the method comprising:

performing word-level implication;

performing ATPG justification on the control signals of the target circuit; and

solving the data signals utilizing a modular constraint solver.

12. The method of Claim 11, wherein the word-level implication comprises a decision on at least one control signal.

13. The method of Claim 12, wherein the word-level implication is performed on some of the one or more control signals and some of the one or more datapath signals.

14. The method of Claim 11, wherein solving the data signals comprises:

extracting one or more arithmetic functions based on the ATPG justification, the one or more arithmetic functions defines the data signals; and

solving the one or more arithmetic functions using the modular constraint solver.

15. A computer-readable storage medium having stored thereon computer instructions that, when executed by a computer, cause the computer to:

provide a representation of a circuit, the representation comprising a control logic component and a datapath logic component;

read one or more vector generation targets;

perform word-level ATPG justification on the control logic component to obtain a control logic solution;

extract one or more arithmetic functions for the datapath logic component based on the control logic solution; and

solve the one or more arithmetic functions using a modular constraint solver, the modular constraint solver being based on a modular number system.

16. The computer-readable storage medium of Claim 15, wherein the computer instructions that perform word-level ATPG justification further comprise computer instructions that, when executed by a computer, cause the computer to perform word-level implication on circuit components related to the one or more targets.

17. The computer-readable storage medium of Claim 15, wherein the computer instructions that solve the one or more arithmetic functions further comprise computer instructions that, when executed by a computer, cause the computer to:

determine possible solutions for the one or more nonlinear equations; and

solve the one or more linear equations using one possible solution for the one or more nonlinear equations as boundary conditions.

18. The computer-readable storage medium of Claim 15, wherein the computer instructions that solve the one or more arithmetic functions further comprise computer instructions that, when executed by a computer, cause the computer to:

dependent on the outcome of solving the one or more arithmetic functions, backtrack to perform word-level ATPG justification on the control logic component to obtain a second control logic solution;

extract one or more arithmetic functions for the datapath logic component based on the second control logic solution; and

solve the one or more arithmetic functions using the modular constraint solver.

19. The computer-readable storage medium of Claim 15, wherein the vector generation target comprises a signal value.

20. The computer-readable storage medium of Claim 15, wherein the vector generation target comprises a relation among a set of signals.

21. The computer-readable storage medium of Claim 15, wherein the vector generation target comprises a sequence of relations among a set of signals.

22. A computer-readable storage medium having stored thereon computer instructions that, when executed by a computer, cause the computer to:

determine a target circuit;

identify an internal control signal of the target circuit;

make a decision on the identified internal control signal;

perform word-level implication on circuit components related to the target circuit;

determine if a conflict arises from the word-level implication; and

determine if the one or more control signals are justified.

23. The computer-readable storage medium of Claim 22, wherein the computer instructions that determine if a conflict arose further comprise computer instructions that, when executed by a computer, cause the computer to:

in response to determining that a conflict arose, backtrack to the previous decision on the identified internal control signal; and

undo the word-level implication associated with the previous decision.

24. The computer-readable storage medium of Claim 22, wherein the computer instructions that determine if the one or more control signals are justified further comprise computer instructions that, when executed by a computer, cause the computer to:

in response to determining that the one or more control signals are not justified, identify a second internal control signal of the target circuit;

make a decision on the identified second internal control signal;

perform word-level implication on circuit components related to the target circuit;

determine if a conflict arises from the word-level implication; and

determine if the one or more control signals are justified.

25. A computer-readable storage medium having stored thereon computer instructions that, when executed by a computer, cause the computer to:

determine a target circuit, the target circuit comprising one or more control signals and one or more data signals;

perform word-level implication;

perform ATPG justification on the control signals of the target circuit; and

solve the data signals utilizing a modular constraint solver.

26. The computer-readable storage medium of Claim 25, wherein the word-level implication comprises a decision on at least one control signal.

27. The computer-readable storage medium of Claim 26, wherein the word-level implication is performed on some of the one or more control signals and some of the one or more datapath signals.

28. The computer-readable storage medium of Claim 25, wherein the computer instructions that solve the data signals further comprise computer instructions that, when executed by a computer, cause the computer to:

extract one or more arithmetic functions based on the ATPG justification, the one or more arithmetic functions defines the data signals; and

solve the one or more arithmetic functions using the modular constraint solver.